Claim Amendments:

Please cancel claims 1-5, 8, and 10.

Please amend claims 6, 7, 9, and 11-14 as follows:

Claims 1-5 (Cancelled)

6. (Currently Amended) A method of fabricating a semiconductor transistor comprising the steps of:

providing a gate structure having a sidewall portion and a top portion, said gate structure formed on a substrate;

forming a dielectric spacer formed over the substrate, said dielectric spacer forming an L-shape comprising a vertical portion parallel to the sidewall portion, and a horizontal portion approximately orthogonal to the sidewall portion of the gate structure;

forming a first source/drain region in the substrate during a source/drain implant using an implant species, selected from the group of indium and antimony, wherein the first source/drain region formed underneath the horizontal portion of the L-shaped dielectric spacer; and

forming a second source/drain region in the substrate during the source/drain implant using the implant species, wherein the second source/drain region is immediately adjacent the first source/drain region and has a depth greater than a depth of the first source/drain region.

7. (Currently Amended) The method of ~~Claim~~ claim 6, further including a step of forming a liner oxide over said gate structure prior to the step of forming the dielectric spacer.

8. (Cancelled)

9. (Currently Amended) The method of ~~Claim~~ claim 6, wherein an ion implantation energy for a boron implant is in the range from approximately 5 keV to 15 keV and ion dose is in the range from about le13/cm^2 to le15/cm^2.

10. (Cancelled)

11. (Currently Amended) The method of ~~Claim~~ claim 6, wherein the ion implantation energy for an arsenic implant in the range of from about 10 keV to about 100 keV and ion dose is in the range from about le13/cm^2 to le15/cm^2.

12. (Currently Amended) The method of ~~Claim~~ claim 6 wherein said L-shaped dielectric spacer is a nitride.

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13. (Currently Amended) The method of ~~Claim~~ claim 6 wherein the length of the horizontal portion of the L-shaped dielectric spacer ranges from about 200 Angstroms to about 500 angstroms.

14. (Currently Amended) A method of fabricating a semiconductor transistor comprising the steps of:

forming a source/drain extension having an average extension depth

forming a first portion of a source/drain region having a first average depth and a first length; and

forming a second portion of the source/drain region simultaneously in time with the first portion, wherein the second portion has a second average depth and a second length, wherein the second average depth is greater than the first average depth, and the first average depth is greater than the average extension depth.